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EXAMINER	
PETRANEK, JACOB ANDREW	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 08/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/743,121	ALBEROLA ET AL.	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5-9 and 11-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-9 and 11-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/11/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-2, 5-9, and 11-24 are pending.

2. The office acknowledges the following papers:

Drawings, claims, arguments, and specification filed on 6/26/2006.

Withdrawn objections

3. The drawing objections for claims 7 and 20 have been withdrawn.

4. The specification objections have been withdrawn due to amendments and clarification.

5. The 35 USC § 112 second paragraph rejections for claim 3 has been withdrawn due to the cancellation of the claim.

6. The 35 USC § 101 rejection for claims 16-17 have been withdrawn due to amendments.

New Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 1-2, 5-9, and 11-24 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1, 8, 16, 18-19, and 21 recite the limitation "partially pre-decoding the instruction at a direct memory access unit." The term partially is unclear in this context.

A pre-decoded instruction is inherently partially decoded. It's unclear how a partially pre-decoded instruction is any different from a pre-decoded instruction. For examination purposes, the term "partially" before pre-decoded will be ignored.

9. Claims 2, 5-7, 9, 11-15, 17, 20, and 22-24 are rejected due to their dependency.

New Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

11. Claims 1-2, 5-9, 11, and 13-20 are rejected under 35 U.S.C. §102(e) as being anticipated by Kotani et al. (U.S. 6,789,140).

12. As per claim 1:

Kotani disclosed a method, comprising:

Retrieving an instruction from a memory unit (Kotani: Figure 9 element 20, column 10 lines 25-48)(The DMA unit receives drawing data and commands from main memory to transfer to the processing unit.);

Pre-decoding the instruction at a direct memory access unit (Kotani: Figure 9 element 234, column 11 lines 51-64)(The DMA pre-decodes instructions in order to look

for interrupts before transferring the instructions and data to the processing unit.); and

Providing the pre-decoded instruction from the direct memory access unit to a processing element (Kotani: Figure 9 element 232, column 10 lines 34-48 and column 11 lines 51-64)(The DMA pre-decodes instructions in order to look for interrupts before transferring the instructions and data to the processing unit, either directly or through the local memory element 40 in figure 9.).

Completely decoding the pre-decoded instruction at the processing element (Kotani: Figure 9 element 232, column 10 lines 34-48)(It's inherent that the processing element fully decodes the command instruction in order to know how the instructions are supposed to operate in the drawing unit.); and

Executing the decoded instruction via a processor pipeline (Kotani: Figure 9 element 232, column 10 lines 34-48)(The drawing unit inherently executes the instructions it receives.).

13. As per claim 2:

Kotani disclosed the method of claim 1, wherein said providing comprises storing the pre-decoded instruction in memory local to the processing element (Kotani: Figure 9 element 40, column 10 lines 34-48 and column 11 lines 51-64)(The DMA pre-decodes instructions in order to look for interrupts before transferring the instructions and data to the processing unit, either directly or through the local memory element 40 in figure 9.).

14. As per claim 5:

Kotani disclosed the method of claim 1, further comprising:

Loading instructions into the memory unit during a boot-up process (Official

notice is taken that instructions are loaded into a memory unit during a boot-up process.).

15. As per claim 6:

Kotani disclosed the method of claim 1, wherein the processing element is a reduced instruction set computer device (Official notice is taken that the processing element could be modified to run a RISC processor architecture.).

16. As per claim 7:

Kotani disclosed the method of claim 6, wherein the pre-decoded instruction comprises execution control signals (Kotani: Figure 11 element 241-242, column 11 lines 29-40)(The DMA unit pre-decodes interrupts and sends control signals back to the host processor.).

17. As per claim 8:

Claim 8 essentially recites the same limitations of claim 1. Therefore, claim 8 is rejected for the same reasons as claim 1.

18. As per claim 9:

Claim 9 essentially recites the same limitations of claim 8. Therefore, claim 9 is rejected for the same reasons as claim 8.

19. As per claim 11:

Claim 11 essentially recites the same limitations of claim 2. Therefore, claim 11 is rejected for the same reasons as claim 2.

20. As per claim 13:

Kotani disclosed the apparatus of claim 8, wherein the input path has n bits, the

output path has q bits, and n < q (Kotani: Figure 11 element 241-242, column 11 lines 29-40)(The DMA unit pre-decodes interrupts and sends control signals back to the host processor. It's inherent that the output path from the DMA must be larger to be able to send out the control signals to the host processor when an interrupt is detected.).

21. As per claim 14:

The apparatus of claim 8, wherein the direct memory access unit, the memory unit, and the processing element are formed on an integrated circuit (Official notice is taken that the DMA, memory, and PE's are formed on an integrated circuit.).

22. As per claim 15:

Claim 15 essentially recites the same limitations of claim 6. Therefore, claim 15 is rejected for the same reasons as claim 6.

23. As per claim 16:

Claim 16 essentially recites the same limitations of claim 1. Therefore, claim 16 is rejected for the same reasons as claim 1.

24. As per claim 17:

Claim 17 essentially recites the same limitations of claim 2. Therefore, claim 17 is rejected for the same reasons as claim 2.

25. As per claim 18:

Kotani disclosed an apparatus, including:

A global memory to store instructions (Kotani: Figure 9 element 20, column 10 lines 25-48)(The DMA unit receives drawing data and commands from main memory to transfer to the processing unit.);

An instruction pre-decoder (Kotani: Figure 9 element 234, column 11 lines 51-64)(The DMA contains a pre-decoder that pre-decodes instructions in order to look for interrupts before transferring the instructions and data to the processing unit.); and

A processor, wherein the instruction pre-decoder is to pre-decode an instruction as it is being transferred from the global memory to the processor (Kotani: Figure 9 element 234, column 11 lines 51-64)(The DMA unit processes instructions before they are sent to the processing unit.), wherein the processor is to completely decode a pre-decoded instruction (Kotani: Figure 9 element 232, column 10 lines 34-48)(It's inherent that the processing element completely decodes the command instruction in order to know how the instructions are supposed to operate in the drawing unit.).

26. As per claim 19:

Kotani disclosed the apparatus of claim 18, further comprising:

A direct memory access unit to arrange for the instruction to be received from the global memory unit and to arrange for a pre-decoded instruction to be provided to the processor (Kotani: Figure 9 element 234, column 11 lines 51-64)(The DMA unit receives instructions from main memory and pre-decodes them to look for interrupts before sending instructions to either the processing unit or local memory.).

27. As per claim 20:

Claim 20 essentially recites the same limitations of claim 7. Therefore, claim 20 is rejected for the same reasons as claim 7.

New Claim Rejections - 35 USC § 103

28. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

29. Claim 12 is rejected under 35 U.S.C. §103(a) as being unpatentable over Kotani et al. (U.S. 6,789,140), in view of Kessler et al. (U.S. 6,738,836).

30. As per claim 12:

Kotani disclosed the apparatus of claim 10, including a plurality of processing elements, each processing element being associated with a direct memory access unit that includes an instruction pre-decoder (Kotani: Figure 9 elements 232 and 234, column 10 lines 34-48 and column 11 lines 51-64).

Kotani failed to teach a plurality of processing elements.

However, Kessler disclosed including a plurality of processing elements (Kessler: Figure 1 element 100, column 4 lines 32-50)(Figure 1 shows a plurality of processing elements that the single processing element of Kotani could be arranged in.).

The advantage of using a large number of processing elements in parallel is that they are able to solve complex computational problems in a reasonable amount of time (Kessler: Column 2 lines 6-14). One of ordinary skill in the art at the time of the invention would have been motivated to implement a parallel computing machine comprised of processing elements of Kotani for the benefits of increased performance. Thus, one of ordinary skill in the art at the time of the invention would have made the

processing element of Kotani into many elements of a large parallel computing structure for the advantage of increased performance.

31. Claim 21 is rejected under 35 U.S.C. §103(a) as being unpatentable over Kotani et al. (U.S. 6,789,140), in view of Ramsdale et al. (U.S. 5,265,263).

32. As per claim 21:

Claim 21 essentially recites the same limitations of claim 1. Claim 21 additionally recites the following limitations:

Kotani failed to teach a multi-directional antenna.

However, Ramsdale disclosed a multi-directional antenna (Ramsdale: Figures 1a and 1b, element 1, column 2 lines 4-13).

The advantage of having a multi-directional antenna is that it allows wireless communication between devices. One of ordinary skill in the art would have been motivated to add a multi-directional antenna to allow for wireless communication between devices. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement a multi-directional antenna to allow for the processor of Kotani to have the ability to communicate wirelessly.

33. Claims 22-23 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kotani et al. (U.S. 6,789,140), in view of Ramsdale et al. (U.S. 5,265,263), further in view of Funderbunk et al. (U.S. 5,291,525)

34. As per claim 22:

Kotani and Ramsdale disclosed the system of claim 21.

Kotani and Ramsdale failed to teach wherein the apparatus is a digital base band processor.

However, Funderbunk disclosed wherein the apparatus is a digital base band processor (Funderbunk: Figure 1, column 3 lines 50-67 continued to column 4 lines 1-37).

Base band is a method of signal transmission. The advantage of using base band is that it has a simple implementation because the signals are transmitted without frequency divisions. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the processor as a digital base band processor for the advantage of a simple implementation of transmitting signals.

35. As per claim 23:

The system of claim 22, wherein the digital base band processor is formed as a system on a chip (Official notice is given that a processor can be formed as a system on a chip.).

36. Claim 24 is rejected under 35 U.S.C. §103(a) as being unpatentable over Kotani et al. (U.S. 6,789,140), in view of Ramsdale et al. (U.S. 5,265,263), further in view of Dent (U.S. 6,229,796).

37. As per claim 24:

Kotani and Ramsdale disclosed the system of claim 21, wherein the system is a time-divisional multiple access base station (Ramsdale: Column 2 lines 39-48)

Kotani and Ramsdale failed to teach wherein the system is a code-division multiple access base station.

However, Dent disclosed wherein the system is a code-division multiple access base station (Dent: Figure 7, column 9 lines 64-67 continued to column 10 lines 1-32).

Both time and code divisional multiple access base station are a ways of allocating frequencies among a plurality of base stations. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention that code-divisional multiple access base station could have been substituted for time-divisional multiple access base station.

Response to Arguments

38. The arguments presented by Applicant in the response, received on 6/26/2006 are not considered persuasive.

39. Applicant argues that "Kotani doesn't disclose a DMA unit that partially pre-decodes instructions."

This argument is not found to be persuasive for the following reason. The term partially has not been examined due to the 112, second paragraph rejection.

40. Applicant argues that "Kotani doesn't disclose completely decoding pre-decoded instructions."

This argument is not found to be persuasive for the following reason. It's inherent that the processing element completely decodes the command instruction in order to know how the instructions are supposed to operate in the drawing unit.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jacob Petranek
Examiner
Art Unit 2183

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